Research and development of new Front-end Electronics for KamLAND2

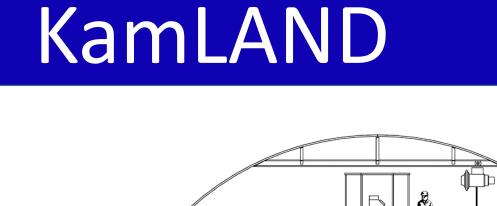
Takeshi Nakahata

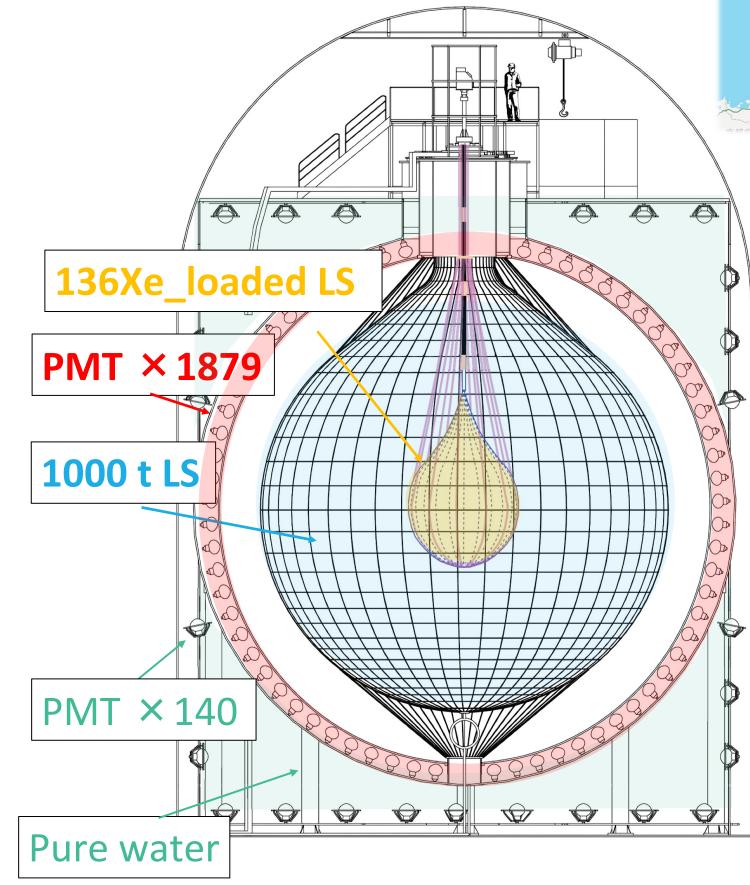
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Research Center for Neutrino Science

Tohoku University **P33**









KamLAND detector

- At 1000 m underground in Kamioka-mine.
- Neutrino detection in **ultra low radioactive** environment

KamLAND2

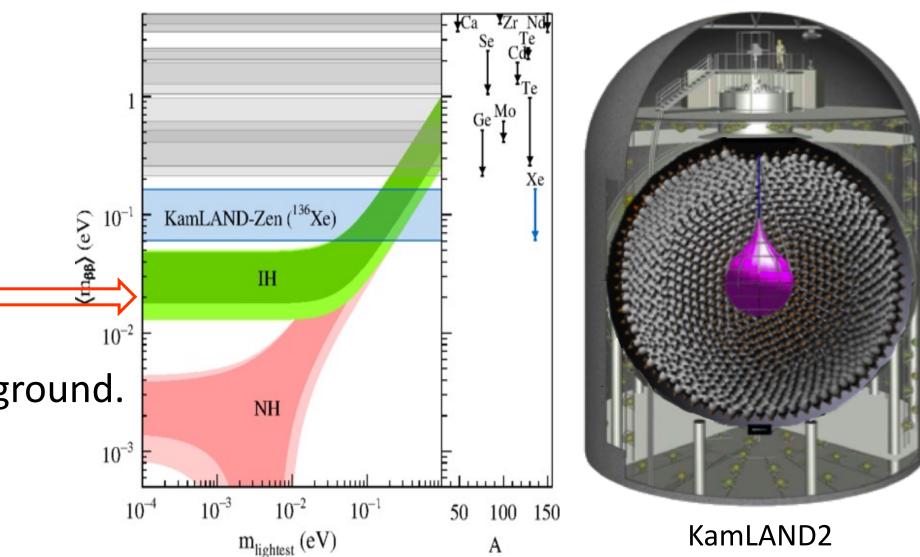
- **1 kt liquid scintillator**
- Measurement of the scintillation light with 1879 PMTs

2ν2β 0ν2β

Majorana nature of neutrino

- KamLAND searches for the neutrino-less double beta (0vββ) decay
- 0vββ is the only realistic way to verify whether
- neutrinos are Majorana particles or Dirac particles.
- KamLAND uses of 745 kg xenon enriched in 136Xe

KamLAND2



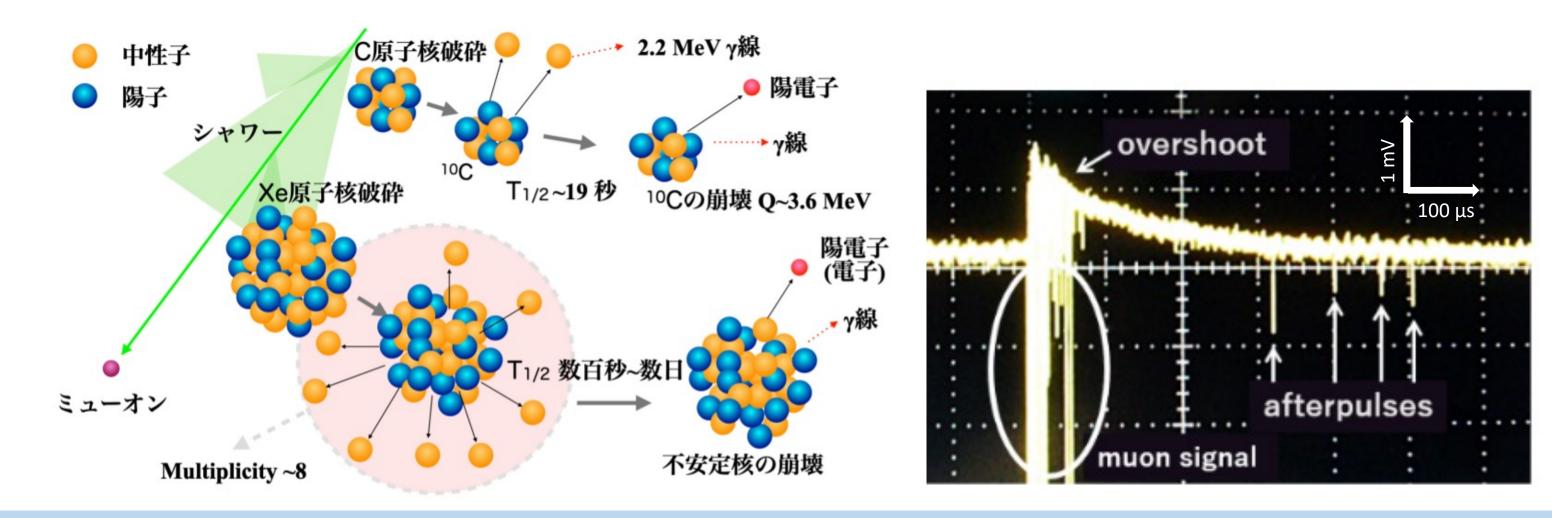
- KamLAND2 is a future plan with better energy resolution against $2v2\beta$ background.
- The goal of KamLAND2 is to reach the sensitivity which covers IH.
- Many R & Ds are ongoing such as <u>new FEE</u>, DAQ, LS, mirror, balloon.

Motivation for new FEE

Detection of all the neutron events caused by spallation products

- The number of neutrons created by the spallation products is an important parameter.
- PMTs make overshoot and afterpulses when muons incidents on the LS.
- We need to detect all the neutron events but it is difficult for KamLAMD, because of the small size of the buffer on the electronics.

Radio Frequency System-on-Chip (RFSoC) based front-end electronics



RFSoC based Front-end Electronics

- Xilinx Zynq[®]Ultrascale+[™] RFSoC is the latest FPGA family from Xilinx,
- which involves ADC, DAC and CPU.
- We can develop the FEE speedily and use the resource of the latest FPGA.
- **DDR4** is for the large on-board buffer.
- Each analog input is divided into two gain channels, **H-gain** and **L-gain**.

	KamLAND	KamLAND2
The number of channels	12	16
Board size	9U (366.7 mm	× 400.0 mm)
FPGA clock	50 MHz	125 MHz
FPGA built-in memory	1.26 MB	7.5 MB
On-board buffer	64 MB	4 GB (DDR4)
Data transfer	VME bass	Ethernet

	Power circuit
	Analog circuit
	KamLAND DS-BD-MoGURA2-1.0.00 A091003 AP9Z-4863A
-	

	H-gain	L-gain
Target	1 – 50 p.e.	Muon
ADC	RF-ADC	ADS42LB69

Sampling rate	1 Gs/s	250 Ms/s
Resolution	12 bit	16 bit

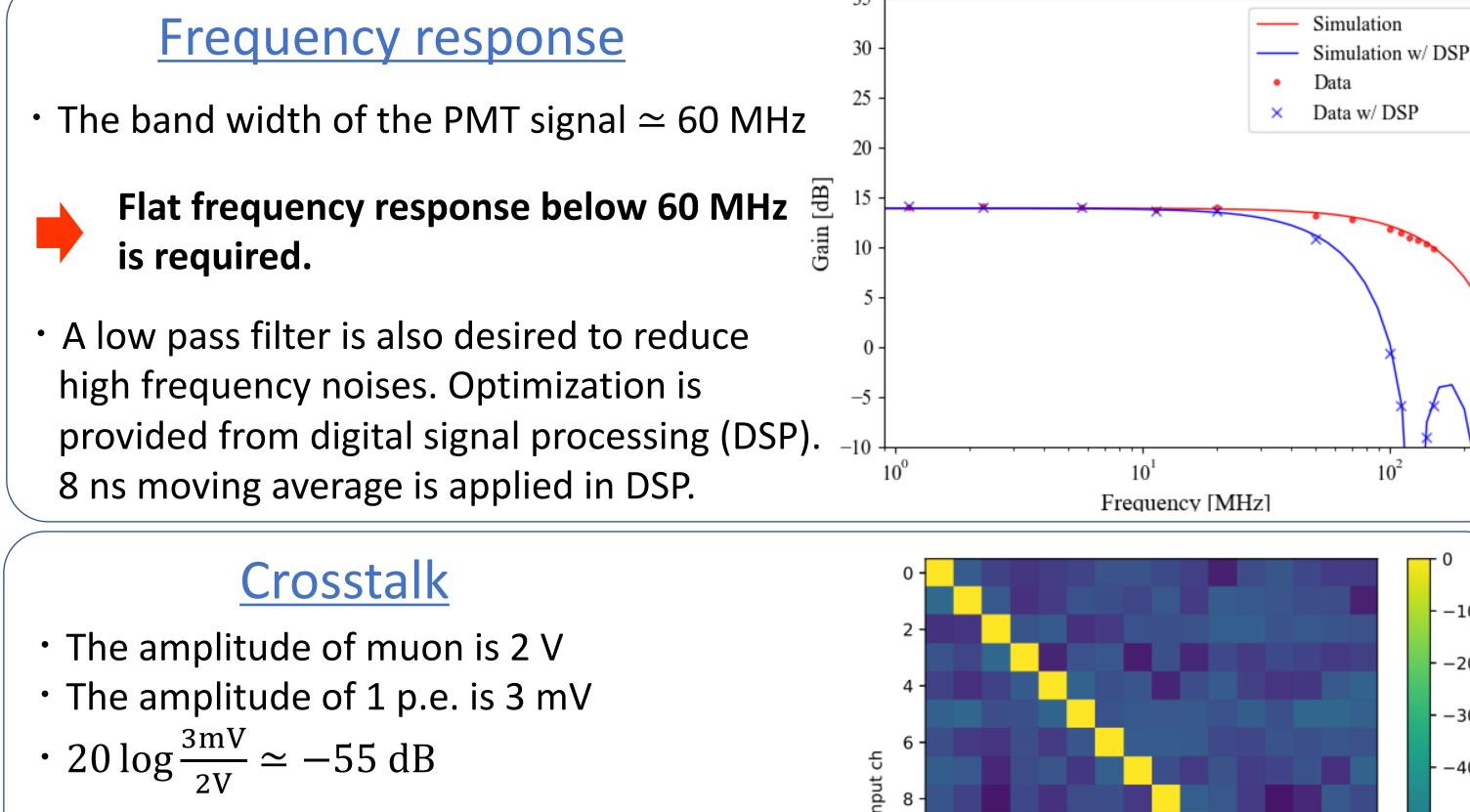
Basic performance evaluation

• We focus on H-gain channel and evaluate the basic performance of 6 items.

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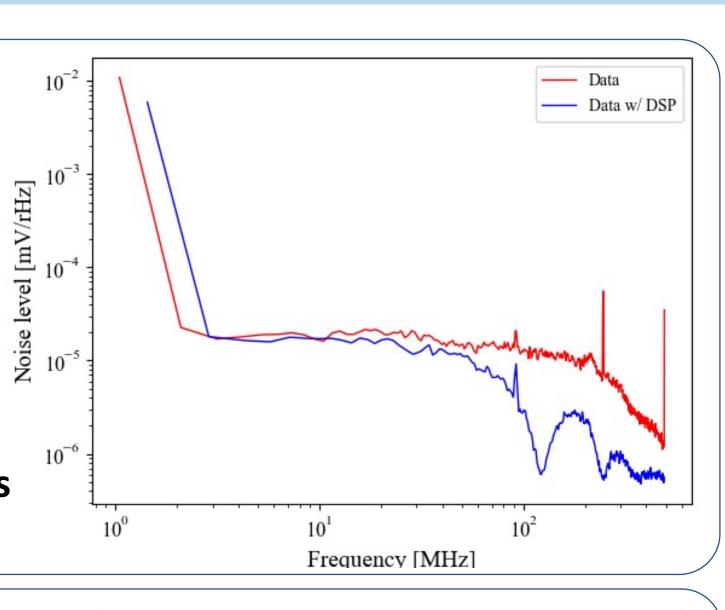


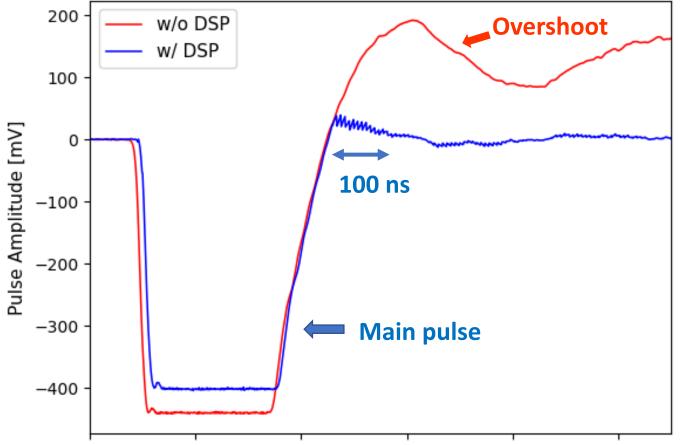
Noise level

- The high frequency noises might prevent detecting single photoelectrons.
- The amplitude of 1 p.e. is 3 mV.
 - **Required noise level for input** equivalent < 0.3 mVrms
- The noise level we measured is **0.17 mVrms**

Baseline correction

- Baseline is restored during overshoot by on-board signal processing.
- We validate the baseline correction function implemented in the DSP module.
- We measured the time for restoring baseline after a large light signal into a PM7
- We confirmed that the baseline correction





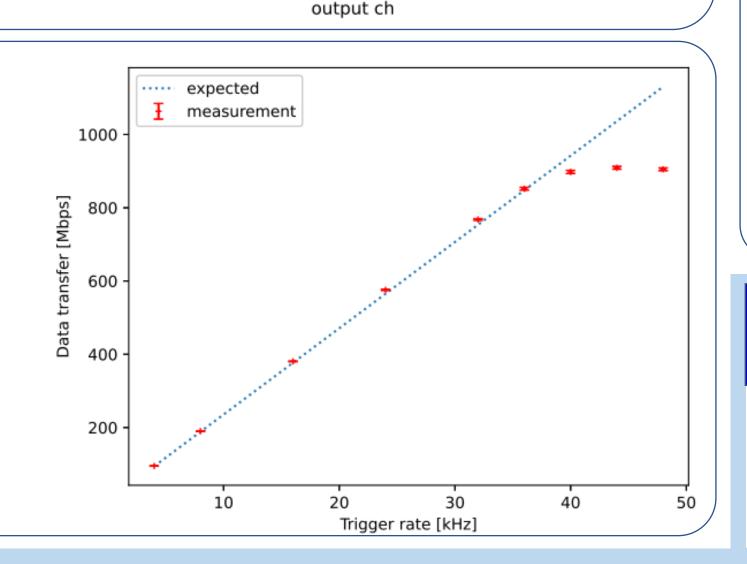
Time [ns]

The crosstalk should be smaller than -55 dB not to generate fake single photoelectrons.

• We measured the amplitude of all channels when inputting sine waves each channel.

Data transfer

- The length of one event is 80 ns \rightarrow 184 byte • Dark rate of PMT is typically 20 kHz • 184 byte \times 20 kHz \times 16 ch \simeq 600 Mbps
- The data transfer speed should be more than 600 Mbps
- We evaluated the data transfer speed with external triggers.



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- -10

- -20

- - 30

-40 <u>m</u>

- -50

- -60

-70

-80

does not alter the PMT signal waveform.

Continuous data acquisition

- We need to record all the waveforms including afterpulses and neutrons signals by the large buffer.
 - Acquiring the continuous waveform data for 10 µs is required.

Summary and Next step

- RFSoC based Front-end Electronics is being developed for KsmLAND2.
- H-gain performances of RFSoC based FEE meets our requirements for KamLAND2.

6ch)

We are developing L-gain for muon and we will test the performance of it.

UGAP2022 2022 6/13 -15 @Tokyo University of Science

Time (us)

34 us